IN THE CLAIMS

Please amend the claims to read as follows:

Listing of Claims

Claims 1-20 (Canceled).

21. (Currently Amended) A method of manufacturing a heterojunction field effect transistor, the method comprising:

epitaxially forming a composite substrate, having a plurality of semiconductor layers on a semi-insulative substrate, the semiconductor layers including a semiconductor layer that serves as an active layer and at least one other semiconductor layer, formed over the upper side or both over the upper side and under the lower side of said active layer, that serves as an N-type carrier supply layer for supplying an electron to said active layer;

diffusing F atoms on the surface of the epitaxial substrate;

forming a gate electrode on said composite substrate; and

forming N-type source and drain areas, by carrying out:

ion injection for forming N-type semiconductors in predetermined areas of said composite substrate, each of said source and drain areas formed to one side of said gate electrode, and

an annealing process for activating the ion injected areas, wherein:

said upper-side N-type carrier supply layer, between said source area and said drain area, is doped with Selenium (Se) or Tellurium (Te), or

at least one of said upper- and lower-side N-type carrier supply layers, between said source area and said drain area, is doped with Selenium (Se) or Tellurium (Te).

22. (Previously Presented) The manufacturing method of claim 21, wherein:

said active layer is formed of InGaAs, and

said upper-side N-type carrier supply layer is formed of AlGaAs or at least one of said upper- and lower-side N-type carrier supply layers is formed of AlGaAs.

23. (Previously Presented) The manufacturing method of claim 21, wherein:

said active layer is formed of InGaAs, and

said upper-side N-type carrier supply layer is formed of InAlAs or at least one of said upper- and lower-side N-type carrier supply layers is formed of InAlAs.

24. (Previously Presented) The manufacturing method of claim 21, wherein:

said active layer is formed of GaAs, and

said upper-side N-type carrier supply layer is formed of AlGaAs or at least one of said upper- and lower-side N-type carrier supply layers is formed of AlGaAs.

25. (Currently Amended) A method of manufacturing a heterojunction field effect transistor, the method comprising:

epitaxially forming a composite substrate, having a plurality of semiconductor layers on a semi-insulative substrate, said plurality of semiconductor layers including a semiconductor layer that serves as an N-type active layer;

diffusing F atoms on the surface of the epitaxial substrate;

forming a gate electrode on said composite substrate; and

forming N-type source and drain areas, by carrying out:

ion injection for forming N-type semiconductors in predetermined areas of said composite substrate, each of said source and drain areas formed to one side of said gate electrode, and

an annealing process for activating the ion injected areas, wherein:

when forming said composite substrate, said semiconductor layer serving as said N-type active layer is doped with Selenium (Se) or Tellurium (Te).

26. (Previously Presented) The method of claim 25, wherein said N-type active layer is an InGaAs layer, a GaAs layer, or an InP layer.

27. (Previously Presented) The method of claim 21, wherein the annealing process for activating the ion injected areas is carried out in a manner of lamp annealing.

28. (Previously Presented) The method claim 25, wherein the annealing process for activating the ion injected areas is carried out in a manner of lamp annealing.

29. (New) The method claim 21, wherein the annealing temperature is in the range of 700°C to 850°C.

30. (New) The method claim 25, wherein the annealing temperature is in the range of 700°C to 850°C.